



IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Peter J. Fricke et al

Confirmation N.:

Application No.: 10/650895

Examiner: Jung H. Hur

Filing Date: Aug 25, 2003

Group Art Unit: 2824

Title: Cubic Memory Array

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

under 37 CFR 1.97 (c) together with either a:
 Statement under 37 CFR 1.97(e), or
 a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

under 37 CFR 1.97 (d) together with a:
 Statement under 37 CFR 1.97(e)(1) or (2), and
 a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account 08-2025 the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: 10/11/03
OR

Respectfully submitted,

Peter J. Fricke et al

By Timothy F. Myers

Timothy F. Myers

Attorney/Agent for Applicant(s)
Reg. No. 42,919

Date: 10/11/03

Typed Name: Timothy F. Myers

Signature: Timothy F. Myers

Telephone No.: 541 715 4197


PATENT APPLICATION

Sheet 1 of 3

FORM PTO-1449

**LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT**

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
10018228-4	10/650,895	
APPLICANT		
Peter J. Fricke et al		
FILING DATE	GROUP	
Aug 25, 2003	2824	

REFERENCE DESIGNATION
U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	3,271,591	Sep 06, 1961	Ovshinsky	
	1B	3,530,441	Sep 22, 1970	Ovshinsky	
	1C	3,641,516	Feb 08, 1972	Castrucci et al	
	1D	4,499,557	Feb 12, 1985	Holmberg et al	
	1E	4,599,705	Jul 08, 1986	Holmberg et al	
	1F	5,335,219	Aug 02, 1994	Ovshinsky et al	
	1G	5,625,220	Apr 29, 1997	Liu et al	
	1H	5,659,500	Aug 19, 1997	Mehrad	
	1I	5,751,012	May 12, 1998	Wolstenholme et al	
	1J	5,821,558	Oct 13, 1998	Han et al	
	1K	5,835,396	Nov 10, 1998	Zhang	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

1Q	Victor, W.C. Chan et al "Multiple Layers of CMOS Integrated Circuits Using Recrystallized Silicon Film" IEEE Electron Device Letters, V. 22(2), Feb. 2001, pp 77-79
1R	Thomas H. Lee, "A Vertical Leap for Microchips," Scientific American, Jan 2002, pp 53-59
1S	Esmat Hamdy et al, "Dielectric based antifuses for logic and memory ICs" IEEE International Electron Devices Meeting, IEDM 88, Aug 1988, pp 786-789

EXAMINER

DATE CONSIDERED



PATENT APPLICATION

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FORM PTO-1449

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ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
10004803-2	10/632,721	
APPLICANT		
Vladek P. Kasperchik et al		
FILING DATE	GROUP	
Aug 01, 2003		

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

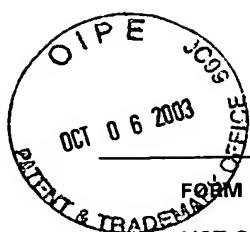
EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
2A	5,942,777	Aug 24, 1999	Chang	
2B	6,002,607	Dec 14, 1999	Dvir	
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2E	6,111,302	Aug 29, 2000	Zhang et al	
2F	6,185,121B1	Feb 06, 2001	O'Neill	
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2H	6,033,955	Mar 07, 2000	Kuo et al	
2I	01/0011776A1	Aug 09 2001	Igarashi et al	
2J	01/0055838A1	Dec 27, 2001	Walker et al	
2K	6,351,406B1	Feb 26, 2002	Johnson et al	

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	2L					
	2M					
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

2Q	Chenming Hu, "Interconnect devices for field programmable gate array." IEEE International Electron Devices Meeting, IEDM 92 (Apr 1992, pp 591-594)
2R	Jonathan Green et al, "Antifuse Field Programmable Gate Arrays", Proc IEEE Vol. 81(7), July 1993, pp 1042-1056.
2S	Vivek D. Kulkarni et al, "Patterning of Submicron Metal Features and Pillars in Multil vel Metallization", J. Electrochem. Soc. V.135(12), Dec. 1988, pp 2094-3098.
EXAMINER	DATE CONSIDERED



PATENT APPLICATION

Sheet 3 of 3

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EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
3A	5,969,380	Oct 1999	Seyyedy	
3B				
3C				
3D				
3E				
3F				
3G				
3H				
3I				
3J				
3K				

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3L					
3M					
3N					
3O					
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

3Q	
3R	
3S	

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